Claims

[c1] 1. A radiation resistant hexagonal gate flash memory cell, comprising:
a substrate;
a source region inside the substrate;
a drain region inside the substrate; and
a gate structure over the substrate between the source region and the drain region, wherein the gate structure further includes an oxide-nitride-oxide layer and a control gate layer sequentially stacked over the substrate such that the gate structure has a hexagonal profile when viewed from the top, and electron-hole pairs generated through a radiation illumination are injected into the substrate.

[c2] 2. The flash memory cell of claim 1, wherein size of both the source region and the drain region are almost identical.

[c3] 3. A radiation resistant flash memory cell, comprising:
a substrate;
a source region inside the substrate;
a drain region inside the substrate, wherein a channel is formed in the substrate between the drain region and the source region; and
a gate structure over the substrate between the source region and the drain region, wherein the gate structure further includes an oxide-nitride-oxide layer and a control gate layer sequentially stacked over the substrate, and in a direction perpendicular to the channel, width of the gate structure increases gradually from the source region towards a pre-determined location and decreases thereafter towards the drain region, and electron-hole pairs generated through a radiation illumination are injected into the substrate.

[c4] 4. The flash memory cell of claim 3, wherein size of both the source region and the drain region is almost identical.

[c5] 5. The flash memory cell of claim 3, wherein the pre-determined location is roughly at a symmetrical line that runs across the central region of the gate structure.

[c6] 6. A radiation resistant flash memory cell, comprising:

a substrate;

a source region inside the substrate;

a drain region inside the substrate, wherein a channel is formed in the substrate between the drain region and the source region; and

a gate structure over the substrate between the source region and the drain region, wherein the gate structure further includes an oxide-nitride-oxide layer over the substrate, and in a direction perpendicular to the channel, width of the gate structure increases gradually from the source region towards a pre-determined location and decreases thereafter towards the drain region;

wherein electron-hole pairs generated through a radiation illumination are injected into the substrate, and in a programming operation, a portion of the gate structure close to the source region serves as an equivalent source region such that overall size of the equivalent source region is greater than the drain region to prevent second bit effect.

[c7] 7. The flash memory cell of claim 6, wherein size of both the source region and the drain region is almost identical.

[c8] 8. The flash memory cell of claim 6, wherein the pre-determined location is roughly at a symmetrical line that runs across the central region of the gate structure.

[c9] 9. The flash memory cell of claim 6, wherein the gradual widening along a direction perpendicular to the channel towards the pre-determined location and narrowing back towards the drain region produces a roughly hexagonal structure.

[c10] 10. A radiation resistant flash memory cell, comprising:

a substrate;

a source region inside the substrate;

a drain region inside the substrate, wherein a channel is formed in the substrate between the drain region and the source region; and

a gate structure over the substrate between the source region and the drain region, wherein the gate structure further includes an oxide-nitride-oxide layer

over the substrate, and in a direction perpendicular to the channel, width of the gate structure is greater than both the source region and the drain region; wherein electron-hole pairs generated through a radiation illumination are injected into the substrate, and in a programming operation, a portion of the gate structure close to the source region serves as an equivalent source region such that overall size of the equivalent source region is greater than the drain region to prevent second bit effect.

[c11] 11. The flash memory cell of claim 10, wherein size of both the source region and the drain region are almost identical.

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